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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/064,767	08/15/2002	Sung-Hung Li	8677-US-PA	9684

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
BENSON, WALTER	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 11/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/064,767	Applicant(s) LI ET AL.
	Examiner Walter Benson	Art Unit 2858 MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-13 and 16-18* is/are rejected.

7)☒ Claim(s) *4,5,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-18 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 6-7, 8-11, and 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Mesuda et al. (US Patent No. 5,563,921 and Mesuda hereinafter).

4. As to claims 1, 8, and 16, Mesuda discloses a signal jitter measuring device for quantifying jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, where the phase locked loop provides a first phase difference signal and a second phase difference signal, the measuring device comprising:
a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between the output signal and the input signal of the phase locked loop (17, Fig. 1; col. 7, lines 11-13);

a jitter-level output unit coupled to the phase-relationship detection unit and responsive to the first phase difference signal, the second phase difference signal and the phase relationship signal for generating a jitter-level output signal that corresponds to the level of jitter between the output signal and the input signal of the phase locked loop (17, 18, Fig. 1; col. 7, lines 13-17 and col. 8, lines 36-39);

where the jitter-level output signal is a pulse width difference between the first phase difference signal and the second phase difference signal (col. 7, lines 41-54).

5. As to claims 6, 9, and 17, Mesuda discloses a signal jitter measuring device for quantifying jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, where the phase locked loop provides a first phase difference signal and a second phase difference signal, the measuring device comprising:

where the first phase difference signal is asserted at the data transition points of the input signal and de-asserted at the next trigger transition point of the output signal after the generation of the second phase difference signal, and the second phase difference signal is asserted at the next non-triggered transition point of the output signal after the data transition of the input signal, and the second phase difference signal is maintained for a full cycle of the output signal (Fig. 3; col. 7, lines 30-40).

6. As to claims 7, 10, and 18, Mesuda discloses a signal jitter measuring device for quantifying jitter between an input signal fed into a phase locked loop and a corresponding

output signal from the phase locked loop, where the phase locked loop provides a first phase difference signal and a second phase difference signal, the measuring device comprising:

where the first phase difference signal is asserted at the triggering transition points of the input signal when the phase of the input signal leads the output signal and de-asserted at subsequent triggering transition points of the output signal, and the second phase difference signal is asserted at the triggering transition points of the output signal when the input signal lags behind the output signal and de-asserted at subsequent triggering transition points of the input signal (col. 7, lines 20-29).

7. As to claim 11, Mesuda discloses a signal jitter measuring device for quantifying jitter between an input signal fed into a phase locked loop and a corresponding output signal from the phase locked loop, where the phase locked loop provides a first phase difference signal and a second phase difference signal, the measuring device further comprising:

a phase-relationship detection unit for outputting a phase relationship signal that corresponds to the phase relationship between the output signal and the input signal of the phase locked loop (col. 8, lines 14-17);

a fitter-level output unit coupled to said phase-relationship detection unit and responsive to the first phase difference signal, said second phase difference signal and the phase relationship signal for generating said fitter-level output signal (17, 18, Fig. 1; col. 7, lines 55-59).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-3, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mesuda as applied to claims 1 and 8 above, and further in view of Pisipaty (US Patent No. 6,628,112 B2 and Pisipaty hereinafter).

Although the system disclosed by Mesuda shows substantial features of the claimed invention (discussed above), it fails to disclose:

where the phase-relationship detection unit comprises:

a triggering unit responsive to said input signal of said phase locked loop for generating triggering signal [claims 2, 12];

a D-type flip-flop taking the output signal of the phase locked loop as its input data and said triggering signal as its input clock to produce the phase relationship signal [claims 2, 12];

where the triggering unit includes:

a delay circuit for delaying said input signal to produce a delayed input signal [claims 3, 13];

a XOR gate for receiving said input signal and said delayed input signal and

producing the triggering signal [claims 3, 13].

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Mesuda, as evidenced by Pisipaty.

In an analogous art, Pisipaty discloses a phase detection circuit including:

where the phase-relationship detection unit comprises:

a triggering unit responsive to said input signal of the phase locked loop for generating triggering signal [claims 2, 12] (402, 404, Fig. 4, col. 5, lines 10-11);

a D-type flip-flop taking the output signal of the phase locked loop as its input data and the triggering signal as its input clock to produce the phase relationship signal [claims 2, 12] (col. 5, lines 11-17) which prevents timing errors;

where the triggering unit includes:

a delay circuit for delaying said input signal to produce a delayed input signal [claims 3, 13] (col. 7, lines 15-18) col. 7, lines 15-18);

a XOR gate for receiving said input signal and said delayed input signal and producing the triggering signal [claims 3, 13] (col. 7, lines 52-54) to allow operation at higher frequencies.

Given the teaching of Pisipaty, a person having ordinary skill in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Mesuda by employing the well known or conventional features of timing functions, such as disclosed by Pisipaty , in order to operate at higher frequencies without additional circuitry.

Allowable Subject Matter

10. Claims 4-5, and 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record fails to teach or suggest individually or in combination an apparatus and method wherein the fitter-level output unit includes a first multiplexer for receiving the first phase difference signal, the second phase difference signal and the phase relationship signal. Then selectively outputting the second phase difference signal when the phase relationship signal indicates the phase of the output signal leads the input signal. Also selectively outputting the first phase difference signal when the phase relationship signal indicates the phase of the output signal lags behind the input signal. A second multiplexer for receiving the first phase difference signal, the second phase difference signal and the phase relationship signal. Then selectively outputting the first phase difference signal when the phase relationship signal indicates the phase of the output signal leads the input signal. Also selectively outputting the second phase difference signal when the phase relationship signal indicates the phase of the output signal lags behind the input signal. A first low-pass filter for converting the output of the first multiplexer into a first low-pass output signal; a second low-pass filter for converting the output of the second multiplexer into a second low-pass output signal. A subtraction unit for receiving the first low-pass output signal and the second low-pass output signal which computes the pulse width difference between the first phase difference signal and the second phase difference signal and produces the jitter-level output signal.

Prior Art Made of Record

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure

A. Kelkar et al. (US Patent No. 5,828,255) discloses a method and apparatus for analyzing and controlling the state of jitter in a phase lock loop;

B. Yanagisawa et al. (US Patent No. 6,528,982 B1) discloses a method and apparatus for measuring at least one parameter to make jitter between signals easily detectable;

C. West (US Patent No. 6,622,107 B1) discloses an apparatus for jitter measurement.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter Benson whose telephone number is (703) 306-4525. The examiner can normally be reached on Mon to Fri 6:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (703) 308-0750. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4900.

Walter Benson WB
Examiner
November 1, 2003

N. Le
Supervisory Patent Examiner
Technology Center 2800